

## 240pin Registered DDR2 SDRAM DIMMs based on 512 Mb B ver.

This Hynix registered Dual In-Line Memory Module (DIMM) series consists of 512Mb B ver. DDR2 SDRAMs in Fine Ball Grid Array(FBGA) packages on a 240pin glass-epoxy substrate. This Hynix 512Mb B ver. based Registered DDR2 DIMM series provide a high performance 8 byte interface in 133.35mm width form factor of industry standard. It is suitable for easy interchange and addition.

### ORDERING INFORMATION

Part Name	Density	Org.	Component Configuration	Ranks	Parity Support
HYMP564R72BP8-E3/C4	512MB	64Mx72	64Mx8(HY5PS12821BFP)*9	1	X
HYMP564P72BP8-E3/C4/Y5/S5	512MB	64Mx72	64Mx8(HY5PS12821BFP)*9	1	O
HYMP512R72BP8-E3/C4	1GB	128Mx72	64Mx8(HY5PS12821BFP)*18	2	X
HYMP512P72BP8-E3/C4/Y5/S5	1GB	128Mx72	64Mx8(HY5PS12821BFP)*18	2	O
HYMP512R72BP4-E3/C4	1GB	128Mx72	128Mx4(HY5PS12421BFP)*18	1	X
HYMP512P72BP4-E3/C4/Y5/S5	1GB	128Mx72	128Mx4(HY5PS12421BFP)*18	1	O
HYMP525R72BP4-E3/C4	2GB	256Mx72	128Mx4(HY5PS12421BFP)*36	2	X
HYMP525P72BP4-E3/C4/Y5/S5	2GB	256Mx72	128Mx4(HY5PS12421BFP)*36	2	O

#### Note:

1. "P" of part number[8th digit] stands for Parity Registered DIMM.
2. "P" of part number[12th digit] stands for Lead free products.

### SPEED GRADE & KEY PARAMETERS

	E3 (DDR2-400)	C4 (DDR2-533)	Y5 (DDR2-667)	S5 (DDR2-800)	Unit
Speed@CL3	400	400	400	400	Mbps
Speed@CL4	400	533	533	533	Mbps
Speed@CL5	-	-	667	800	Mbps
CL-tRCD-tRP	3-3-3	4-4-4	5-5-5	5-5-5	tCK

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**FEATURES**

- JEDEC standard 1.8V +/- 0.1V Power Supply
- $V_{DDQ}$  : 1.8V +/- 0.1V
- All inputs and outputs are compatible with SSTL\_1.8 interface
- 4 Bank architecture
- Posted  $\overline{\text{CAS}}$
- Programmable CAS Latency 3 , 4 , 5
- OCD (Off-Chip Driver Impedance Adjustment)
- ODT (On-Die Termination)
- Fully differential clock operations (CK &  $\overline{\text{CK}}$ )
- Programmable Burst Length 4 / 8 with both sequential and interleave mode
- Average Auto Refresh Period 7.8us under  $T_{\text{CASE}} = 85^{\circ}\text{C}$ , 3.9us at  $85^{\circ}\text{C} < T_{\text{CASE}} \leq 95^{\circ}\text{C}$
- High Temperature Self-Refresh Entry enableble features
- PASR(Partial Array Self- Refresh)
- 8192 refresh cycles / 64ms
- Serial presence detect with EEPROM
- DDR2 SDRAM Package: 60ball FBGA
- 133.35 x 30.00 mm form factor
- Lead-free Products are RoHS compliant

**ADDRESS TABLE**

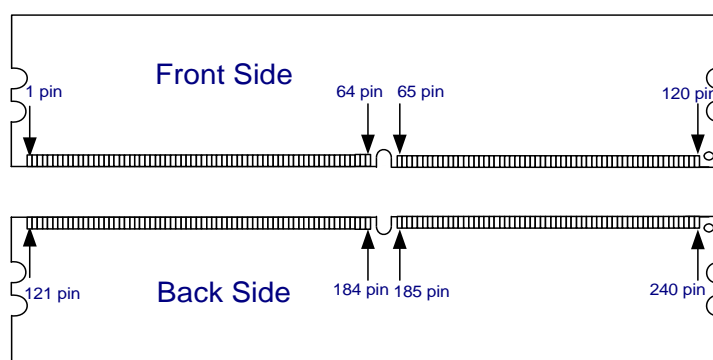
Density	Organization	Ranks	SDRAMs	# of DRAMs	# of row/bank/column Address	Refresh Method
<b>512MB</b>	64M x 72	1	64Mb x 8	9	14(A0~A13)/2(BA0~BA1)/10(A0~A9)	8K / 64ms
<b>1GB</b>	128M x 72	2	64Mb x 8	18	14(A0~A13)/2(BA0~BA1)/10(A0~A9)	8K / 64ms
<b>1GB</b>	128M x 72	1	128Mb x 4	18	14(A0~A13)/2(BA0~BA1)/11(A0~A9,A11)	8K / 64ms
<b>2GB</b>	256M x 72	2	128Mb x 4	36	14(A0~A13)/2(BA0~BA1)/11(A0~A9,A11)	8K / 64ms

**Input/Output Functional Description**

Symbol	Type	Polarity	Pin Description
CK0	IN	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL.
$\overline{CK0}$	IN	Negative Edge	Negative line of the differential pair of system clock inputs that drives input to the on-DIMM PLL.
CKE[1:0]	IN	Active High	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S}[1:0]$	IN	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by S0; Rank 1 is selected by S1
ODT[1:0]	IN	Active High	On-Die Termination signals.
$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	IN	Active Low	When sampled at the positive rising edge of the clock. RAS,CAS and WE(ALONG WITH S) define the command being entered.
Vref	Supply		Reference voltage for SSTL18 inputs
V <sub>DDQ</sub>	Supply		Power supplies for the DDR2 SDRAM output buffers to provide improved noise immunity. For all current DDR2 unbuffered DIMM designs, V <sub>DDQ</sub> shares the same power plane as V <sub>DD</sub> pins.
BA[1:0]	IN	-	Selects which DDR2 SDRAM internal bank of four is activated.
A[9:0], A10/AP A[13:11]	IN	-	During a Bank Activate command cycle, Address input defines the row address(RA0~RA13)  During a Read or Write command cycle, Address input defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$ . In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high., autoprecharge is selected and BA0-BA <sub>n</sub> defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle., AP is used in conjunction with BA0-BA <sub>n</sub> to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BA <sub>n</sub> inputs. If AP is low, then BA0-BA <sub>n</sub> are used to define which bank to precharge.
DQ[63:0], CB[7:0]	IN	-	Data and Check Bit Input/Output pins.
DM[8:0]	IN	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V <sub>DD</sub> ,V <sub>SS</sub>	Supply		Power and ground for the DDR2 SDRAM input buffers, and core logic. V <sub>DD</sub> and V <sub>DDQ</sub> pins are tied to V <sub>DD</sub> /V <sub>DDQ</sub> planes on these modules.
DQS[17:0]	I/O	Positive Edge	Positive line of the differential data strobe for input and output data
$\overline{DQS}$ [17:0]	I/O	Negative Edge	Negative line of the differential data strobe for input and output data
SA[2:0]	IN	-	These signals are tied at the system planar to either V <sub>SS</sub> or V <sub>DDSPD</sub> to configure the serial SPD EEPROM address range.
SDA	I/O	-	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor may be connected from the SDA bus line to V <sub>DDSPD</sub> on the system planar to act as a pull up.
SCL	IN	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V <sub>DDSPD</sub> to act as a pull up on the system board.
VDDSPD	Supply		Power supply for SPD EEPROM. This supply is separate from the VDD/VDDQ power plane. EEPROM supply is operable from 1.7V to 3.6V.
RESET	IN		The RESET pin is connected to the RST pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and register(s) will be set to low level (the PLL will remain synchronized with the input clock)
Par_In	IN		Parity bit for the Address and Control bus("1". Odd, "0".Even)
Err_Out	OUT		Parity error found in the Address and Control bus
TEST			Used by memory bus analysis tools(unused on memory DIMMs)

**PIN DESCRIPTION**

Pin	Pin Description	Pin	Pin Description
CK0	Clock Input,positive line	ODT[1:0]	On Die Termination Inputs
$\overline{\text{CK0}}$	Clock input,negative line	VDDQ	DQs Power Supply
CKE0~CKE1	Clock Enable Input	DQ0~DQ63	Data Input/Output
$\overline{\text{RAS}}$	Row Address Strobe	CB0~CB7	Data check bits Input/Output
$\overline{\text{CAS}}$	Column Address Strobe	DQS(0~8)	Data strobes
$\overline{\text{WE}}$	Write Enable	$\overline{\text{DQS}}(0~8)$	Data strobes,negative line
$\overline{\text{S0}},\overline{\text{S1}}$	Chip Select Input	DM(0~8), DQS(9~17)	Data Maskes/Data strobes
A0~A9, A11~A13	Address input	$\overline{\text{DQS}}(9~17)$	Data strobes,negative line
A10/AP	Address input/Autoprecharge	RFU	Reserved for Future Use
BA0,BA1	SDRAM Bank Address	NC	No Connect
SCL	Serial Presence Detect(SPD) Clock Input	TEST	Memory bus test tool (Not Connected and Not Usable on DIMMs)
SDA	SPD Data Input/Output	VDD	Core Power
SA0~SA2	E <sup>2</sup> PROM Address Inputs	VDDQ	I/O Power
Par_In	Parity bit for the Address and Control bus	VSS	Ground
Err_Out	Parity error found on the Address	VREF	Input/Output Reference
$\overline{\text{RESET}}$	Reset Enable	VDDSPD	SPD Power
CB0~CB7	Data Check bit Inputs/Outputs		

**PIN LOCATION**


**PIN ASSIGNMENT**

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	41	VSS	81	DQ33	121	VSS	161	CB4	201	VSS
2	VSS	42	CB0	82	VSS	122	DQ4	162	CB5	202	DM4/DQS13
3	DQ0	43	CB1	83	$\overline{\text{DQS4}}$	123	DQ5	163	VSS	203	$\overline{\text{DQS13}}$
4	DQ1	44	VSS	84	DQS4	124	VSS	164	DM8,DQS17	204	VSS
5	VSS	45	$\overline{\text{DQS8}}$	85	VSS	125	DM0/DQS9	165	$\overline{\text{DQS17}}$	205	DQ38
6	$\overline{\text{DQS0}}$	46	DQS8	86	DQ34	126	$\overline{\text{DQS9}}$	166	VSS	206	DQ39
7	DQS0	47	VSS	87	DQ35	127	VSS	167	CB6	207	VSS
8	VSS	48	CB2	88	VSS	128	DQ6	168	CB7	208	DQ44
9	DQ2	49	CB3	89	DQ40	129	DQ7	169	VSS	209	DQ45
10	DQ3	50	VSS	90	DQ41	130	VSS	170	VDDQ	210	VSS
11	VSS	51	VDDQ	91	VSS	131	DQ12	171	NC,CKE1	211	DM5/DQS14
12	DQ8	52	CKE0	92	$\overline{\text{DQS5}}$	132	DQ13	172	VDD	212	$\overline{\text{DQS14}}$
13	DQ9	53	VDD	93	DQS5	133	VSS	173	A15,NC	213	VSS
14	VSS	54	BA2,NC	94	VSS	134	DM1/DQS10	174	A14,NC	214	DQ46
15	$\overline{\text{DQS1}}$	55	NC,Err_Out	95	DQ42	135	$\overline{\text{DQS10}}$	175	VDDQ	215	DQ47
16	DQS1	56	VDDQ	96	DQ43	136	VSS	176	A12	216	VSS
17	VSS	57	A11	97	VSS	137	RFU	177	A9	217	DQ52
18	$\overline{\text{RESET}}$	58	A7	98	DQ48	138	RFU	178	VDD	218	DQ53
19	NC	59	VDD	99	DQ49	139	$\overline{\text{VSS}}$	179	A8	219	VSS
20	VSS	60	A5	100	VSS	140	DQ14	180	A6	220	RFU
21	DQ10	61	A4	101	SA2	141	DQ15	181	VDDQ	221	RFU
22	DQ11	62	VDDQ	102	NC(TEST)	142	VSS	182	A3	222	VSS
23	VSS	63	A2	103	VSS	143	DQ20	183	A1	223	DM6/DQS15
24	DQ16	64	VDD	104	$\overline{\text{DQS6}}$	144	DQ21	184	VDD	224	NC, $\overline{\text{DQS15}}$
25	DQ17	Key		105	DQS6	145	VSS	Key		225	VSS
26	VSS	65	VSS	106	VSS	146	DM2/DQS11	185	CK0	226	DQ54
27	$\overline{\text{DQS2}}$	66	VSS	107	DQ50	147	$\overline{\text{DQS11}}$	186	$\overline{\text{CK0}}$	227	DQ55
28	DQS2	67	VDD	108	DQ51	148	VSS	187	VDD	228	VSS
29	VSS	68	NC,Err_Out	109	VSS	149	DQ22	188	A0	229	DQ60
30	DQ18	69	VDD	110	DQ56	150	DQ23	189	VDD	230	DQ61
31	DQ19	70	A10/AP	111	DQ57	151	VSS	190	BA1	231	VSS
32	VSS	71	BA0	112	VSS	152	DQ28	191	VDDQ	232	DM7/DQS16
33	DQ24	72	VDDQ	113	$\overline{\text{DQS7}}$	153	DQ29	192	$\overline{\text{RAS}}$	233	NC, $\overline{\text{DQS16}}$
34	DQ25	73	$\overline{\text{WE}}$	114	DQS7	154	VSS	193	$\overline{\text{S0}}$	234	VSS
35	VSS	74	$\overline{\text{CAS}}$	115	VSS	155	DM3/DQS12	194	VDDQ	235	DQ62
36	$\overline{\text{DQS3}}$	75	VDDQ	116	DQ58	156	$\overline{\text{DQS12}}$	195	ODT0	236	DQ63
37	DQS3	76	NC, $\overline{\text{S1}}$	117	DQ59	157	VSS	196	A13,NC	237	VSS
38	VSS	77	NC, ODT1	118	VSS	158	DQ30	197	VDD	238	VDDSPD
39	DQ26	78	VDDQ	119	SDA	159	DQ31	198	VSS	239	SA0
40	DQ27	79	VSS	120	SCL	160	VSS	199	DQ36	240	SA1
		80	DQ32					200	DQ37		

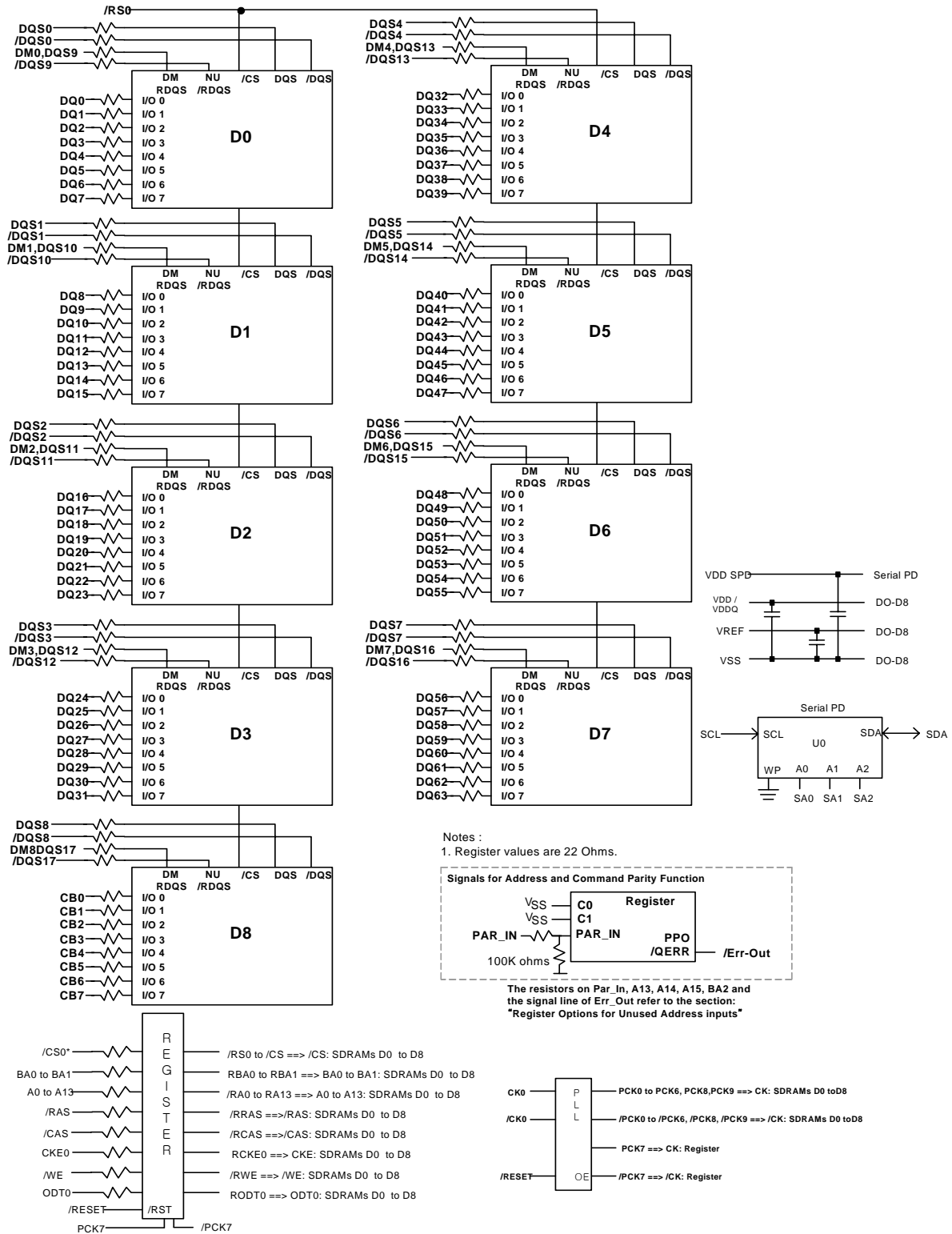
NC= No Connect, RFU= Reserved for Future Use.

**Note:**

1. RESET(Pin 18) is connected to both OE of PLL and Reset of register.
2. NC/Err\_out (Pin 55) and NC/Par\_In(Pin68) are for optional function to check address and command parity.
3. The Test pin(Pin 102) is reserved for bus analysis probes and is not connected on normal memory modules(DIMMs)

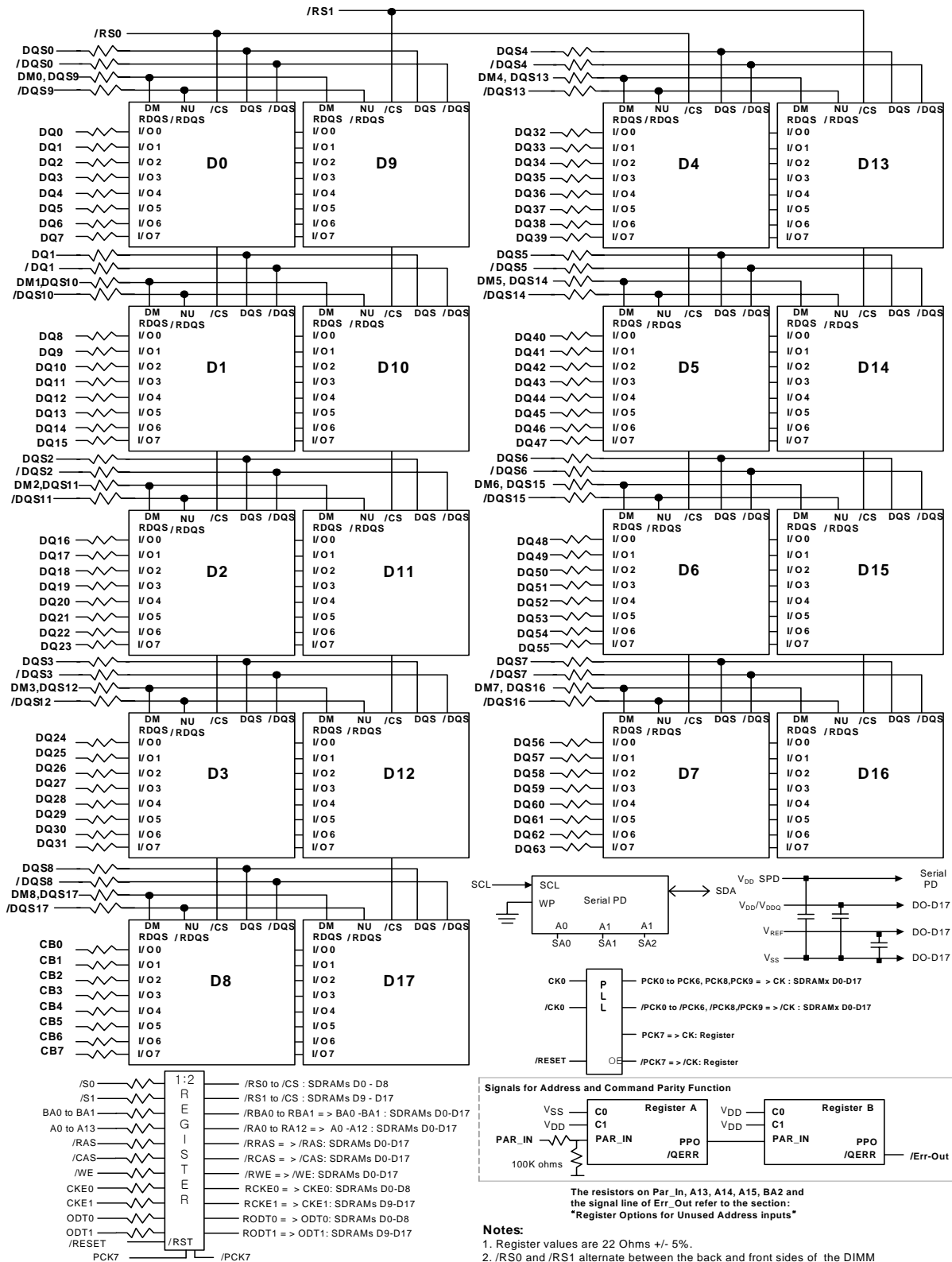
FUNCTIONAL BLOCK DIAGRAM

512MB(64Mbx72) : HYMP564R72BP8 / HYMP564P72BP8



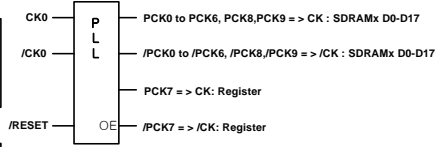
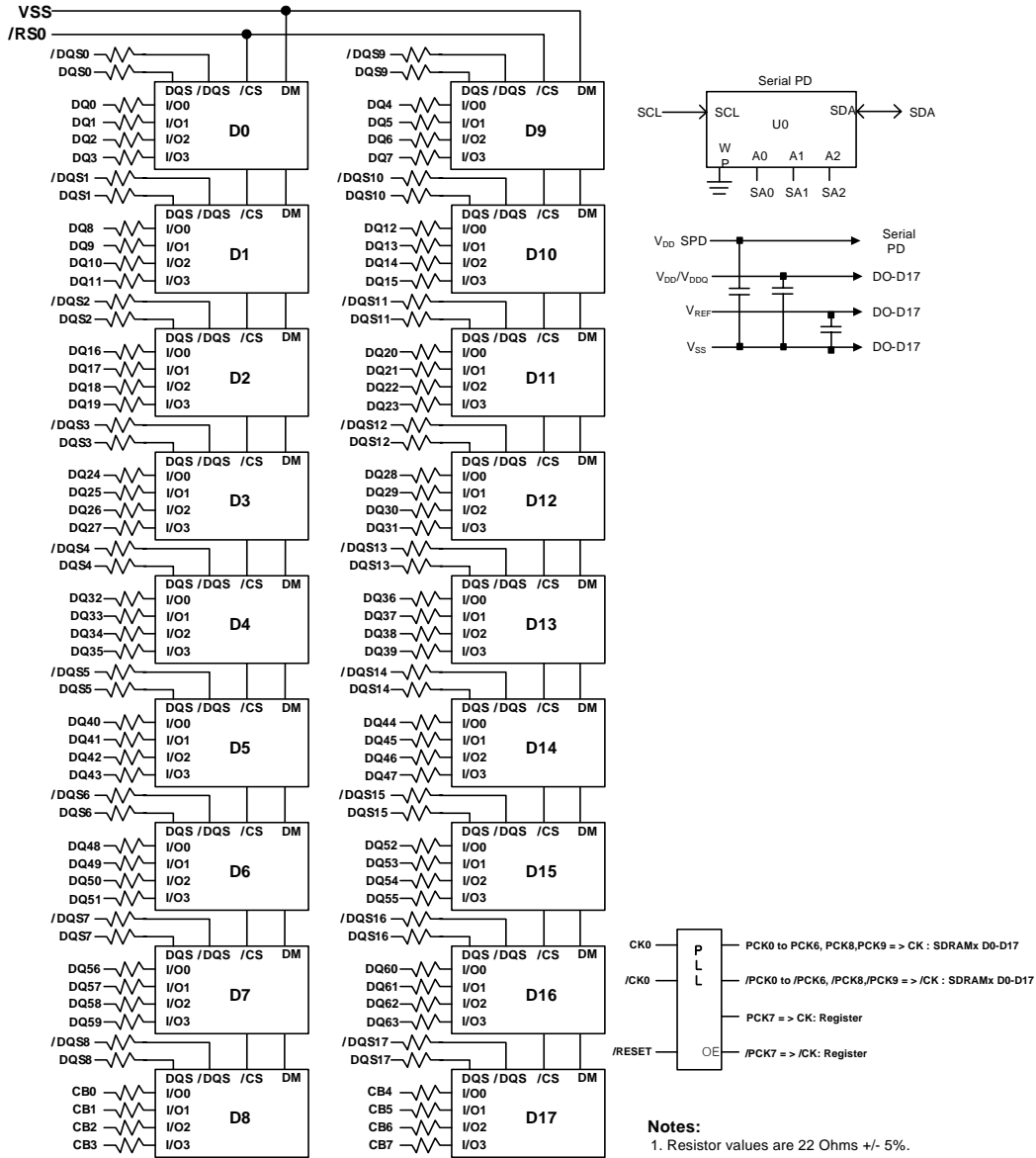
## FUNCTIONAL BLOCK DIAGRAM

1GB(128Mbx72) : HYMP512R72BP8 / HYMP512P72BP8

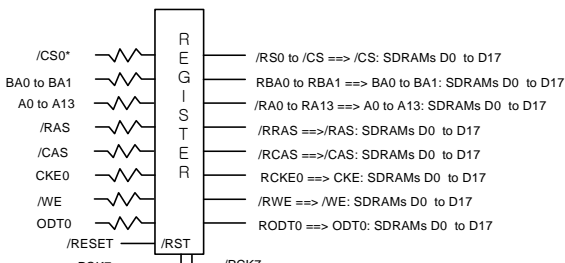


FUNCTIONAL BLOCK DIAGRAM

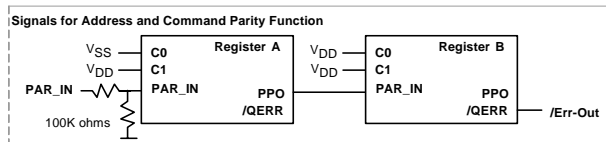
1GB(64Mbx72) : HYMP512R72BP4 / HYMP512P72BP4



**Notes:**  
1. Resistor values are 22 Ohms +/- 5%.



\* /S0 connects to D/CS of Register1 and /CSR of Register2. /CSR of register and D/CS of register2 connects to VDD.  
\*\* /RESET, PCK7 connect to both Registers. Other signals connect to one of two Registers. /S1, CKE1 and ODT1 are NC.

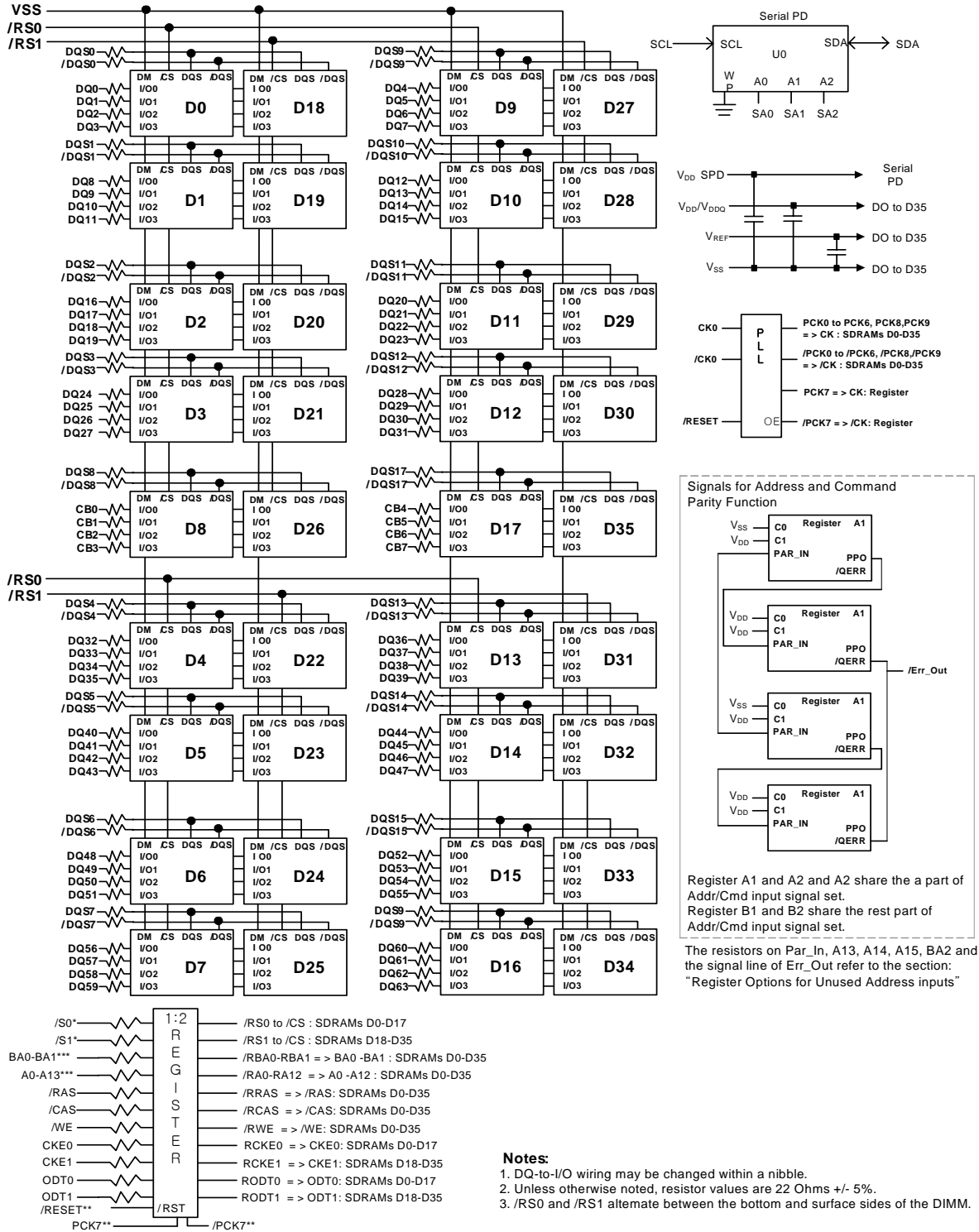


The resistors on Par\_In, A13, A14, A15, BA2 and the signal line of Err\_Out refer to the section: "Register Options for Unused Address inputs"



## FUNCTIONAL BLOCK DIAGRAM

2GB(256Mbx72) : HYMP525R72BP4 / HYMP525P72BP4



\* /S0 connects to D/CS0 and /S1 connects to CSR on a pair of Registers. /S1 connects to D/CS and /S0 connects to /CSR on another pair of Registers.  
 \*\* /RESET, PCK7 and /PCK7 connect to both Registers. Other signals connect to two Registers.  
 \*\*\* A13-15, BA2 have the optional pull down resistors(100k ohms), which is not indicated here.

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit	Note
Voltage on V <sub>DD</sub> pin relative to V <sub>ss</sub>	V <sub>DD</sub>	- 1.0 V ~ 2.3 V	V	1
Voltage on VDDL pin relative to V <sub>ss</sub>	V <sub>DDL</sub>	-0.5V ~ 2.3 V	V	1
Voltage on V <sub>DDQ</sub> pin relative to V <sub>ss</sub>	V <sub>DDQ</sub>	- 0.5 V ~ 2.3 V	V	1
Voltage on any pin relative to V <sub>ss</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	- 0.5 V ~ 2.3 V	V	1
Storage Temperature	T <sub>STG</sub>	-50 ~ +100	°C	1
Storage Humidity(without condensation)	H <sub>STG</sub>	5 to 95	%	1

**Note :**

1. Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING CONDITIONS**

Parameter	Symbol	Rating	Units	Notes
DIMM Operating temperature(ambient)	T <sub>OPR</sub>	0 ~ +55	°C	
DIMM Barometric Pressure(operating & storage)	p <sup>BAR</sup>	105 to 69	K Pascal	1
DRAM Component Case Temperature Range	T <sub>CASE</sub>	0 ~ +95	°C	2

**Note :**

1. Up to 9850 ft.
2. If the DRAM case temperature is Above 85°C, the Auto-Refresh command interval has to be reduced to tREFI=3.9us. For Measurement conditions of T<sub>CASE</sub>, please refer to the JEDEC document JESD51-2.

**DC OPERATING CONDITIONS (SSTL\_1.8)**

Parameter	Symbol	Min	Max	Unit	Note
Power Supply Voltage	V <sub>DD</sub>	1.7	1.9	V	
	V <sub>DDL</sub>	1.7	1.9	V	
	V <sub>DDQ</sub>	1.7	1.9	V	1
Input Reference Voltage	V <sub>REF</sub>	0.49 x V <sub>DDQ</sub>	0.51 x V <sub>DDQ</sub>	V	2
EEPROM Supply Voltage	V <sub>DDSPD</sub>	1.7	3.6	V	
Termination Voltage	V <sub>TT</sub>	V <sub>REF</sub> -0.04	V <sub>REF</sub> +0.04	V	3
Input leakage current; any input 0V VIN VDD; all other balls not under test = 0V)	I <sub>I</sub>	-2	2	uA	
Output leakage current; 0V VOUT VDDQ; DQ and ODT disabled	I <sub>OZ</sub>	-5	5	uA	

**Note :**

1. V<sub>DDQ</sub> must be less than or equal to V<sub>DD</sub>.
2. Peak to peak ac noise on V<sub>REF</sub> may not exceed +/-2% V<sub>REF</sub>(dc)
3. V<sub>TT</sub> of transmitting device must track V<sub>REF</sub> of receiving device.

**INPUT DC LOGIC LEVEL**

Parameter	Symbol	Min	Max	Unit	Notes
Input High Voltage	$V_{IH(DC)}$	$V_{REF} + 0.125$	$V_{DDQ} + 0.3$	V	
Input Low Voltage	$V_{IL(DC)}$	-0.30	$V_{REF} - 0.125$	V	

**INPUT AC LOGIC LEVEL**

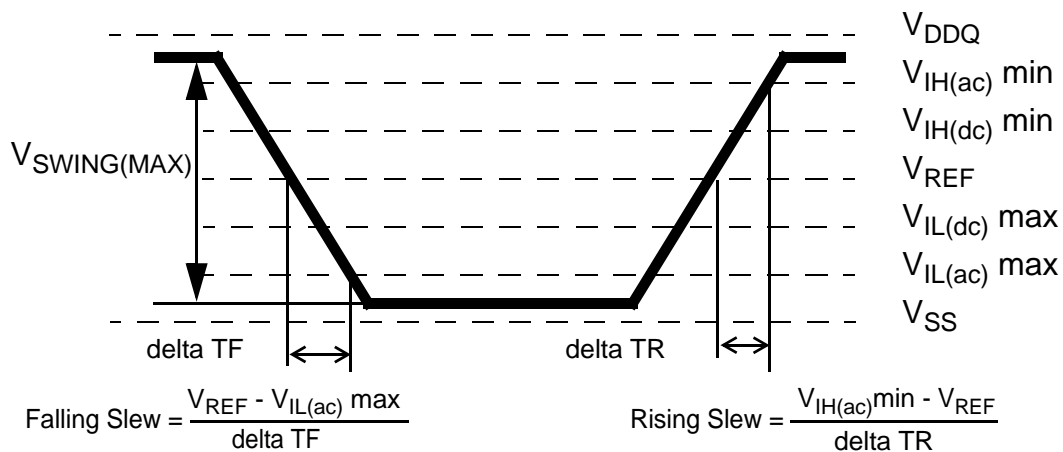
Parameter	Symbol	DDR2 400/533		DDR2 667/800		Unit	Notes
		Min	Max	Min	Max		
AC Input logic High	$V_{IH(AC)}$	$V_{REF} + 0.250$	-	$V_{REF} + 0.200$	-	V	
AC Input logic Low	$V_{IL(AC)}$	-	$V_{REF} - 0.250$	-	$V_{REF} - 0.200$	V	

**AC INPUT TEST CONDITIONS**

Symbol	Condition	Value	Units	Notes
$V_{REF}$	Input reference voltage	$0.5 * V_{DDQ}$	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

**Notes:**

1. Input waveform timing is referenced to the input signal crossing through the  $V_{REF}$  level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from  $V_{REF}$  to  $V_{IH(ac) min}$  for rising edges and the range from  $V_{REF}$  to  $V_{IL(ac) max}$  for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from  $V_{IL(ac)}$  to  $V_{IH(ac)}$  on the positive transitions and  $V_{IH(ac)}$  to  $V_{IL(ac)}$  on the negative transitions.

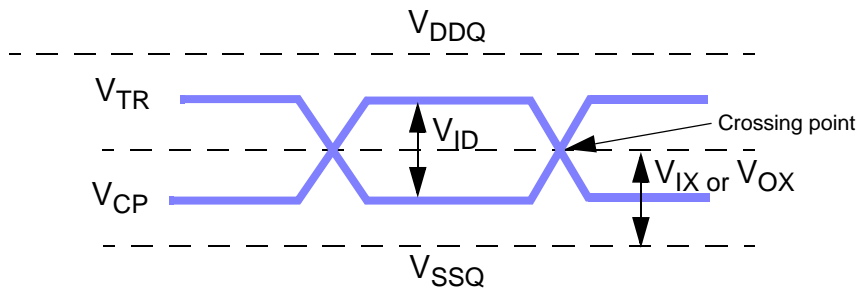


< Figure : AC Input Test Signal Waveform >

### Differential Input AC logic Level

Symbol	Parameter	Min.	Max.	Units	Note
$V_{ID} (ac)$	ac differential input voltage	0.5	$V_{DDQ} + 0.6$	V	1
$V_{IX} (ac)$	ac differential cross point voltage	$0.5 * V_{DDQ} - 0.175$	$0.5 * V_{DDQ} + 0.175$	V	2

- $V_{IN}(DC)$  specifies the allowable DC execution of each input of differential pair such as  $\overline{CK}$ ,  $\overline{DQS}$ ,  $\overline{LDQS}$ ,  $\overline{UDQS}$  and  $\overline{UDQS}$ .
- $V_{ID}(DC)$  specifies the input differential voltage  $|V_{TR} - V_{CP}|$  required for switching, where  $V_{TR}$  is the true input (such as  $\overline{CK}$ ,  $\overline{DQS}$ ,  $\overline{LDQS}$  or  $\overline{UDQS}$ ) level and  $V_{CP}$  is the complementary input (such as  $\overline{CK}$ ,  $\overline{DQS}$ ,  $\overline{LDQS}$  or  $\overline{UDQS}$ ) level. The minimum value is equal to  $V_{IH}(DC) - V_{IL}(DC)$ .



< Differential signal levels >

**Notes:**

- $V_{ID}(AC)$  specifies the input differential voltage  $|V_{TR} - V_{CP}|$  required for switching, where  $V_{TR}$  is the true input signal (such as  $\overline{CK}$ ,  $\overline{DQS}$ ,  $\overline{LDQS}$  or  $\overline{UDQS}$ ) and  $V_{CP}$  is the complementary input signal (such as  $\overline{CK}$ ,  $\overline{DQS}$ ,  $\overline{LDQS}$  or  $\overline{UDQS}$ ). The minimum value is equal to  $V_{IH}(AC) - V_{IL}(AC)$ .
- The typical value of  $V_{IX}(AC)$  is expected to be about  $0.5 * V_{DDQ}$  of the transmitting device and  $V_{IX}(AC)$  is expected to track variations in  $V_{DDQ}$ .  $V_{IX}(AC)$  indicates the voltage at which differential input signals must cross.

### DIFFERENTIAL AC OUTPUT PARAMETERS

Symbol	Parameter	Min.	Max.	Units	Note
$V_{OX} (ac)$	ac differential cross point voltage	$0.5 * V_{DDQ} - 0.125$	$0.5 * V_{DDQ} + 0.125$	V	1

**Note:**

- The typical value of  $V_{OX}(AC)$  is expected to be about  $0.5 * V_{DDQ}$  of the transmitting device and  $V_{OX}(AC)$  is expected to track variations in  $V_{DDQ}$ .  $V_{OX}(AC)$  indicates the voltage at which differential output signals must cross.

## OUTPUT BUFFER LEVELS

### OUTPUT AC TEST CONDITIONS

Symbol	Parameter	SSTL_18	Units	Notes
$V_{OTR}$	Output Timing Measurement Reference Level	$0.5 * V_{DDQ}$	V	1

**Notes:**

1. The VDDQ of the device under test is referenced.

### OUTPUT DC CURRENT DRIVE

Symbol	Parameter	SSTL_18	Units	Notes
$I_{OH(dc)}$	Output Minimum Source DC Current	- 13.4	mA	1, 3, 4
$I_{OL(dc)}$	Output Minimum Sink DC Current	13.4	mA	2, 3, 4

**Notes:**

1.  $V_{DDQ} = 1.7\text{ V}$ ;  $V_{OUT} = 1420\text{ mV}$ .  $(V_{OUT} - V_{DDQ})/I_{OH}$  must be less than 21 ohm for values of  $V_{OUT}$  between  $V_{DDQ}$  and  $V_{DDQ} - 280\text{ mV}$ .
2.  $V_{DDQ} = 1.7\text{ V}$ ;  $V_{OUT} = 280\text{ mV}$ .  $V_{OUT}/I_{OL}$  must be less than 21 ohm for values of  $V_{OUT}$  between 0 V and 280 mV.
3. The dc value of  $V_{REF}$  applied to the receiving device is set to  $V_{TT}$
4. The values of  $I_{OH(dc)}$  and  $I_{OL(dc)}$  are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure  $V_{IH}$  min plus a noise margin and  $V_{IL}$  max minus a noise margin are delivered to an SSTL\_18 receiver.

The actual current values are derived by shifting the desired driver operating point along a 21 ohm load line to define a convenient driver current for measurement.

**PIN Capacitance** (VDD=1.8V, VDDQ=1.8V, TA=25°C, f=1MHz)

**512MB : HYMP564R72BP8 / HYMP564P72BP8**

Pin	Symbol	Min	Max	Unit
CK0, $\overline{\text{CK0}}$	CCK	7	11	pF
CKE, ODT	C11	8	12	pF
$\overline{\text{CS}}$	C12	8	12	pF
Address, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$	C13	8	12	pF
DQ, DM, DQS, $\overline{\text{DQS}}$	C10	6	9	pF

**1GB : HYMP512R72BP8 / HYMP512P72BP8**

Pin	Symbol	Min	Max	Unit
CK0, $\overline{\text{CK0}}$	CCK	7	11	pF
CKE, ODT	C11	8	12	pF
$\overline{\text{CS}}$	C12	10	15	pF
Address, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$	C13	8	12	pF
DQ, DM, DQS, $\overline{\text{DQS}}$	C10	8	13	pF

**1GB : HYMP512R72BP4 / HYMP512P72BP4**

Pin	Symbol	Min	Max	Unit
CK0, $\overline{\text{CK0}}$	CCK	7	11	pF
CKE, ODT	C11	8	12	pF
$\overline{\text{CS}}$	C12	10	15	pF
Address, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$	C13	8	12	pF
DQ, DM, DQS, $\overline{\text{DQS}}$	C10	6	9	pF

**2GB : HYMP525R72BP4 / HYMP525P72BP4**

Pin	Symbol	Min	Max	Unit
CK0, $\overline{\text{CK0}}$	CCK	9.5	10.4	pF
CKE, ODT	C11	10.5	16	pF
$\overline{\text{CS}}$	C12	10.5	16	pF
Address, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$	C13	10.5	16	pF
DQ, DM, DQS, $\overline{\text{DQS}}$	C10	17	21	pF

**Note :**

1. Pins not under test are tied to GND.
2. These value are guaranteed by design and tested on a sample basis only.

**IDD SPECIFICATIONS** ( $T_{CASE}$  : 0 to 95°C)

**512MB, 64M x 72 Registered DIMM : HYMP564R72BP8 / HYMP564P72BP8**

Symbol	E3 (400@CL3)	C4 (533@CL4)	Y5 (667@CL5)	S5 (800@CL5)	Unit	Notes
IDD0	1370	1370	TBD	TBD	mA	
IDD1	1460	1460	TBD	TBD	mA	
IDD2P	722	722	TBD	TBD	mA	
IDD2Q	920	1010	TBD	TBD	mA	
IDD2N	965	1055	TBD	TBD	mA	
IDD3P-F	920	920	TBD	TBD	mA	
IDD3P-S	758	758	TBD	TBD	mA	
IDD3N	1100	1145	TBD	TBD	mA	
IDD4W	1910	2180	TBD	TBD	mA	
IDD4R	1820	2000	TBD	TBD	mA	
IDD5	2090	2180	TBD	TBD	mA	1
IDD6	495	495	TBD	TBD	mA	
IDD7	2630	2630	TBD	TBD	mA	

**1GB, 128M x 72 Registered DIMM : HYMP512R72BP8 / HYMP512P72BP8**

Symbol	E3 (400@CL3)	C4 (533@CL4)	Y5 (667@CL5)	S5 (800@CL5)	Unit	Notes
IDD0	1820	1865	TBD	TBD	mA	
IDD1	1910	1955	TBD	TBD	mA	
IDD2P	794	794	TBD	TBD	mA	
IDD2Q	1190	1370	TBD	TBD	mA	
IDD2N	1280	1460	TBD	TBD	mA	
IDD3P-F	1190	1190	TBD	TBD	mA	
IDD3P-S	866	866	TBD	TBD	mA	
IDD3N	1550	1640	TBD	TBD	mA	
IDD4W	2360	2675	TBD	TBD	mA	
IDD4R	2270	2495	TBD	TBD	mA	
IDD5	2540	2675	TBD	TBD	mA	1
IDD6	540	540	TBD	TBD	mA	
IDD7	3080	3125	TBD	TBD	mA	

**Notes :**

1. IDD6 current values are guaranteed up to Tcase of 85°C max.

**1GB, 128M x 72 Registered DIMM : HYMP512R72BP4 / HYMP512P72BP4**

Symbol	E3 (400@CL3)	C4 (533@CL4)	Y5 (667@CL5)	S5 (800@CL5)	Unit	Notes
IDD0	2090	2090	TBD	TBD	mA	
IDD1	2270	2270	TBD	TBD	mA	
IDD2P	794	794	TBD	TBD	mA	
IDD2Q	1190	1370	TBD	TBD	mA	
IDD2N	1280	1460	TBD	TBD	mA	
IDD3P-F	1190	1190	TBD	TBD	mA	
IDD3P-S	866	866	TBD	TBD	mA	
IDD3N	1550	1640	TBD	TBD	mA	
IDD4W	3170	3710	TBD	TBD	mA	
IDD4R	2990	3350	TBD	TBD	mA	
IDD5	3530	3710	TBD	TBD	mA	1
IDD6	540	540	TBD	TBD	mA	
IDD7	4610	4610	TBD	TBD	mA	

**2GB, 256M x 72 Registered DIMM : HYMP525R72BP4/HYMP525P72BP4**

Symbol	E3 (400@CL3)	C4 (533@CL4)	Y5 (667@CL5)	S5 (800@CL5)	Unit	Notes
IDD0	2990	3080	TBD	TBD	mA	
IDD1	3170	3260	TBD	TBD	mA	
IDD2P	938	938	TBD	TBD	mA	
IDD2Q	1730	2090	TBD	TBD	mA	
IDD2N	1910	2270	TBD	TBD	mA	
IDD3P-F	1730	1730	TBD	TBD	mA	
IDD3P-S	1082	1082	TBD	TBD	mA	
IDD3N	2450	2630	TBD	TBD	mA	
IDD4W	4070	4700	TBD	TBD	mA	
IDD4R	3890	4340	TBD	TBD	mA	
IDD5	4430	4700	TBD	TBD	mA	1
IDD6	630	630	TBD	TBD	mA	
IDD7	5510	5600	TBD	TBD	mA	

**Note :**

1. IDD6 current values are guaranteed up to Tcase of 85°C max.



**IDD Measurement Conditions**

Symbol	Conditions	Units
IDD0	<b>Operating one bank active-precharge current;</b> $t_{CK} = t_{CK}(IDD)$ , $t_{RC} = t_{RC}(IDD)$ , $t_{RAS} = t_{RAS-min}(IDD)$ ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA
IDD1	<b>Operating one bank active-read-precharge current;</b> $I_{OUT} = 0mA$ ; $BL = 4$ , $CL = CL(IDD)$ , $AL = 0$ ; $t_{CK} = t_{CK}(IDD)$ , $t_{RC} = t_{RC}(IDD)$ , $t_{RAS} = t_{RAS-min}(IDD)$ , $t_{RCD} = t_{RCD}(IDD)$ ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA
IDD2P	<b>Precharge power-down current;</b> All banks idle; $t_{CK} = t_{CK}(IDD)$ ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA
IDD2Q	<b>Precharge quiet standby current;</b> All banks idle; $t_{CK} = t_{CK}(IDD)$ ; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA
IDD2N	<b>Precharge standby current;</b> All banks idle; $t_{CK} = t_{CK}(IDD)$ ; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA
IDD3P	<b>Active power-down current;</b> All banks open; $t_{CK} = t_{CK}(IDD)$ ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0
		Slow PDN Exit MRS(12) = 1
IDD3N	<b>Active standby current;</b> All banks open; $t_{CK} = t_{CK}(IDD)$ , $t_{RAS} = t_{RAS-max}(IDD)$ , $t_{RP} = t_{RP}(IDD)$ ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA
IDD4W	<b>Operating burst write current;</b> All banks open, Continuous burst writes; $BL = 4$ , $CL = CL(IDD)$ , $AL = 0$ ; $t_{CK} = t_{CK}(IDD)$ , $t_{RAS} = t_{RAS-max}(IDD)$ , $t_{RP} = t_{RP}(IDD)$ ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA
IDD4R	<b>Operating burst read current;</b> All banks open, Continuous burst reads, $I_{OUT} = 0mA$ ; $BL = 4$ , $CL = CL(IDD)$ , $AL = 0$ ; $t_{CK} = t_{CK}(IDD)$ , $t_{RAS} = t_{RAS-max}(IDD)$ , $t_{RP} = t_{RP}(IDD)$ ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA
IDD5B	<b>Burst refresh current;</b> $t_{CK} = t_{CK}(IDD)$ ; Refresh command at every $t_{RFC}(IDD)$ interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA
IDD6	<b>Self refresh current;</b> CK and $\overline{CK}$ at 0V; CKE $\leq 0.2V$ ; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING. IDD6 current values are guaranteed up to Tcase of 85°C max.	mA
IDD7	<b>Operating bank interleave read current;</b> All bank interleaving reads, $I_{OUT} = 0mA$ ; $BL = 4$ , $CL = CL(IDD)$ , $AL = t_{RCD}(IDD) - 1 * t_{CK}(IDD)$ ; $t_{CK} = t_{CK}(IDD)$ , $t_{RC} = t_{RC}(IDD)$ , $t_{RRD} = t_{RRD}(IDD)$ , $t_{RCD} = 1 * t_{CK}(IDD)$ ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; - Refer to the following page for detailed timing conditions	mA

**Notes:**

1. IDD specifications are tested after the device is properly initialized
2. Input slew rate is specified by AC Parametric Test Condition
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS,  $\overline{DQS}$ , RDQS,  $\overline{RDQS}$ , LDQS,  $\overline{LDQS}$ , UDQS, and  $\overline{UDQS}$ . IDD values must be met with all combinations of EMRS bits 10 and 11.
5. Definitions for IDD
  - LOW is defined as  $V_{in} \leq V_{ILAC}(max)$
  - HIGH is defined as  $V_{in} \geq V_{IHAC}(min)$
  - STABLE is defined as inputs stable at a HIGH or LOW level
  - FLOATING is defined as inputs at  $V_{REF} = V_{DDQ}/2$
  - SWITCHING is defined as: inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

## Electrical Characteristics & AC Timings

Speed Bins and CL,tRCD,tRP,tRC and tRAS for Corresponding Bin

Speed	DDR2-800	DDR2-667	DDR2-533	DDR2-400	Unit
Bin(CL-tRCD-tRP)	5-5-5	5-5-5	4-4-4	3-3-3	
Parameter	min	min	min	min	
CAS Latency	5	5	4	5	ns
tRCD	12.5	15	15	15	ns
tRP	12.5	15	15	15	ns
tRAS	45	45	45	40	ns
tRC	57.25	60	60	55	ns

### AC Timing Parameters by Speed Grade

Parameter	Symbol	DDR2-400		DDR2-533		Unit	Note
		Min	Max	Min	Max		
Data-Out edge to Clock edge Skew	tAC	-600	+600	-500	500	ps	
DQS-Out edge to Clock edge Skew	tDQSK	-500	+500	-500	450	ns	
Clock High Level Width	tCH	0.45	0.55	0.45	0.55	CK	
Clock Low Level Width	tCL	0.45	0.55	0.45	0.55	CK	
Clock Half Period	tHP	min(tCL,tCH)	-	min(tCL,tCH)	-	ns	
System Clock Cycle Time	tCK	5000	8000	3750	8000	ps	
DQ and DM input setup time(differential strobe)	tDS	150	-	100	-	ps	1
DQ and DM input hold time(differential strobe)	tDH	275	-	225	-	ps	1
DQ and DM input setup time(single ended strobe)	tDS1	25	-	-25	-	ps	1
DQ and DM input hold time(single ended strobe)	tDH1	25	-	-25	-	ps	1
Control & Address input Pulse Width for each input	tIPW	0.6	-	0.6	-	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	-	0.35	-	tCK	
Data-out high-impedance window from CK, /CK	tHZ	-	tAC max	-	tAC max	ps	
DQS low-impedance time from CK/ $\overline{CK}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	
DQ low-impedance time from CK/ $\overline{CK}$	tLZ(DQ)	2*tAC min	tAC max	2*tAC min	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	350	-	300	ps	
DQ hold skew factor	tQHS	-	450	-	400	ps	
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	tHP - tQHS	-	ps	
First DQS latching transition to associated clock edge	tDQSS	-0.25	+ 0.25	-0.25	+ 0.25	tCK	
DQS input high pulse width	tDQSH	0.35	-	0.35	-	tCK	
DQS input low pulse width	tDQSL	0.35	-	0.35	-	tCK	
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK	
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	tCK	
Mode register set command cycle time	tMRD	2	-	2	-	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	

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Parameter	Symbol	DDR2-400		DDR2-533		Unit	Note
		Min	Max	Min	Max		
Write preamble	tWPRE	0.35	-	0.35	-	tCK	
Address and control input setup time	tIS	350	-	250	-	ps	
Address and control input hold time	tIH	475	-	375	-	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Auto-Refresh to Active/Auto-Refresh command period	tRFC	105	-	105	-	ns	
Row Active to Row Active Delay for 1KB page size	tRRD	7.5	-	7.5	-	ns	
Four Activate Window for 1KB page size	tFAW	37.5	-	37.5	-	ns	
CAS to CAS command delay	tCCD	2		2		tCK	
Write recovery time	tWR	15	-	15	-	ns	
Auto Precharge Write Recovery + Precharge Time	tDAL	WR+tRP	-	tWR+tRP	-	tCK	
Write to Read Command Delay	tWTR	10	-	7.5	-	ns	
Internal read to precharge command delay	tRTP	7.5		7.5		ns	
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		ns	
Exit self refresh to a read command	tXSRD	200	-	200	-	tCK	
Exit precharge power down to any non-read command	tXP	2	-	2	-	tCK	
Exit active power down to read command	tXARD	2		2		tCK	
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL		6 - AL		tCK	
CKE minimum pulse width (high and low pulse width)	t <sup>'</sup> CKE	3		3		tCK	
ODT turn-on delay	t <sup>'</sup> AOND	2	2	2	2	tCK	
ODT turn-on	t <sup>'</sup> AON	tAC(min)	tAC(max)+1	tAC(min)	tAC(max)+1	ns	
ODT turn-on(Power-Down mode)	t <sup>'</sup> AONPD	tAC(min)+2	2tCK+tAC(max)+1	tAC(min)+2	2tCK+tAC(max)+1	ns	
ODT turn-off delay	t <sup>'</sup> AOFD	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	t <sup>'</sup> AOF	tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	ns	
ODT turn-off (Power-Down mode)	t <sup>'</sup> AOFPD	tAC(min)+2	2.5tCK+tAC(max)+1	tAC(min)+2	2.5tCK+tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT power down exit latency	tAXPD	8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		ns	
Average periodic Refresh Interval	tREFI	-	7.8	-	7.8	us	2
	tREFI	-	3.9	-	3.9	us	3

**Note :**

1. For details and notes, please refer to the relevant HYNIX component datasheet (HY5PS12[4, 8]21BFP).
2. 0°C ≤ TCASE ≤ 85°C
3. 85°C < TCASE ≤ 95°C

Parameter	Symbol	DDR2-667		DDR2-800		Unit	Note
		min	max	min	max		
DQ output access time from CK/ $\overline{\text{CK}}$	tAC	-450	+450	-400	+400	ps	
DQS output access time from CK/ $\overline{\text{CK}}$	tDQSCK	-400	+400	-350	+350	ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL, tCH)	-	min(tCL, tCH)	-	ps	
Clock cycle time, CL=x	tCK	3000	8000	2500		ps	
DQ and DM input setup time (differential strobe)	tDS	100	-	50	-	ps	1
DQ and DM input hold time (differential strobe)	tDH	175	-	125	-	ps	1
Control & Address input pulse width for each input	tIPW	0.6	-	0.6	-	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	-	0.35	-	tCK	
Data-out high-impedance time from CK/ $\overline{\text{CK}}$	tHZ	-	tAC max	-	tAC max	ps	
DQS low-impedance time from CK/ $\overline{\text{CK}}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	
DQ low-impedance time from CK/ $\overline{\text{CK}}$	tLZ(DQ)	2*tAC min	tAC max	2*tAC min	tAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	240	-	200	ps	
DQ hold skew factor	tQHS	-	340	-	300	ps	
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	tHP - tQHS	-	ps	
First DQS latching transition to associated clock edge	tDQSS	- 0.25	+ 0.25	- 0.25	+ 0.25	tCK	
DQS input high pulse width	tDQSH	0.35	-	0.35	-	tCK	
DQS input low pulse width	tDQSL	0.35	-	0.35	-	tCK	
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK	
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	tCK	
Mode register set command cycle time	tMRD	2	-	2	-	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	
Write preamble	tWPRE	0.35	-	0.35	-	tCK	
Address and control input setup time	tIS	200	-	175	-	ps	
Address and control input hold time	tIH	275	-	250	-	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Activate to precharge command	tRAS	45	70000	45	70000	ns	
Active to active command period for 1KB page size products	tRRD	7.5	-	7.5	-	ns	
Four Active Window for 1KB page size products	tFAW	37.5	-	35	-	ns	

- continued -

Parameter	Symbol	DDR2-667		DDR2-800		Unit	Note
		min	max	min	max		
CAS to $\overline{\text{CAS}}$ command delay	tCCD	2		2		tCK	
Write recovery time	tWR	15	-	15	-	ns	
Auto precharge write recovery + precharge time	tDAL	WR+tRP	-	WR+tRP	-	tCK	
Internal write to read command delay	tWTR	7.5	-	7.5	-	ns	
Internal read to precharge command delay	tRTP	7.5		7.5		ns	
Exit self refresh to a non-read command	tXSNR	tRFC + 10		tRFC + 10		ns	
Exit self refresh to a read command	tXSRD	200	-	200	-	tCK	
Exit precharge power down to any non-read command	tXP	2	-	2	-	tCK	
Exit active power down to read command	tXARD	2		2		tCK	
Exit active power down to read command (Slow exit, Lower power)	tXARDS	7 - AL		8 - AL		tCK	
CKE minimum pulse width (high and low pulse width)	t <sub>CKE</sub>	3		3		tCK	
ODT turn-on delay	t <sub>AOND</sub>	2	2	2	2	tCK	
ODT turn-on	t <sub>AON</sub>	tAC(min)	tAC(max) + 0.7	tAC(min)	tAC(max) + 0.7	ns	
ODT turn-on(Power-Down mode)	t <sub>AONPD</sub>	tAC(min) + 2	2tCK + tAC(max) + 1	tAC(min) + 2	2tCK + tAC(max) + 1	ns	
ODT turn-off delay	t <sub>AOFD</sub>	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	t <sub>AOF</sub>	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	ns	
ODT turn-off (Power-Down mode)	t <sub>AOFPD</sub>	tAC(min) + 2	2.5tCK + tAC(max) + 1	tAC(min) + 2	2.5tCK + tAC(max) + 1	ns	
ODT to power down entry latency	tANPD	3		3		tCK	
ODT power down exit latency	tAXPD	8		8		tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		tIS+tCK+tIH		ns	
Average periodic Refresh Interval	tREFI	-	7.8	-	7.8	us	2
	tREFI	-	3.9	-	3.9	us	3

**Note :**

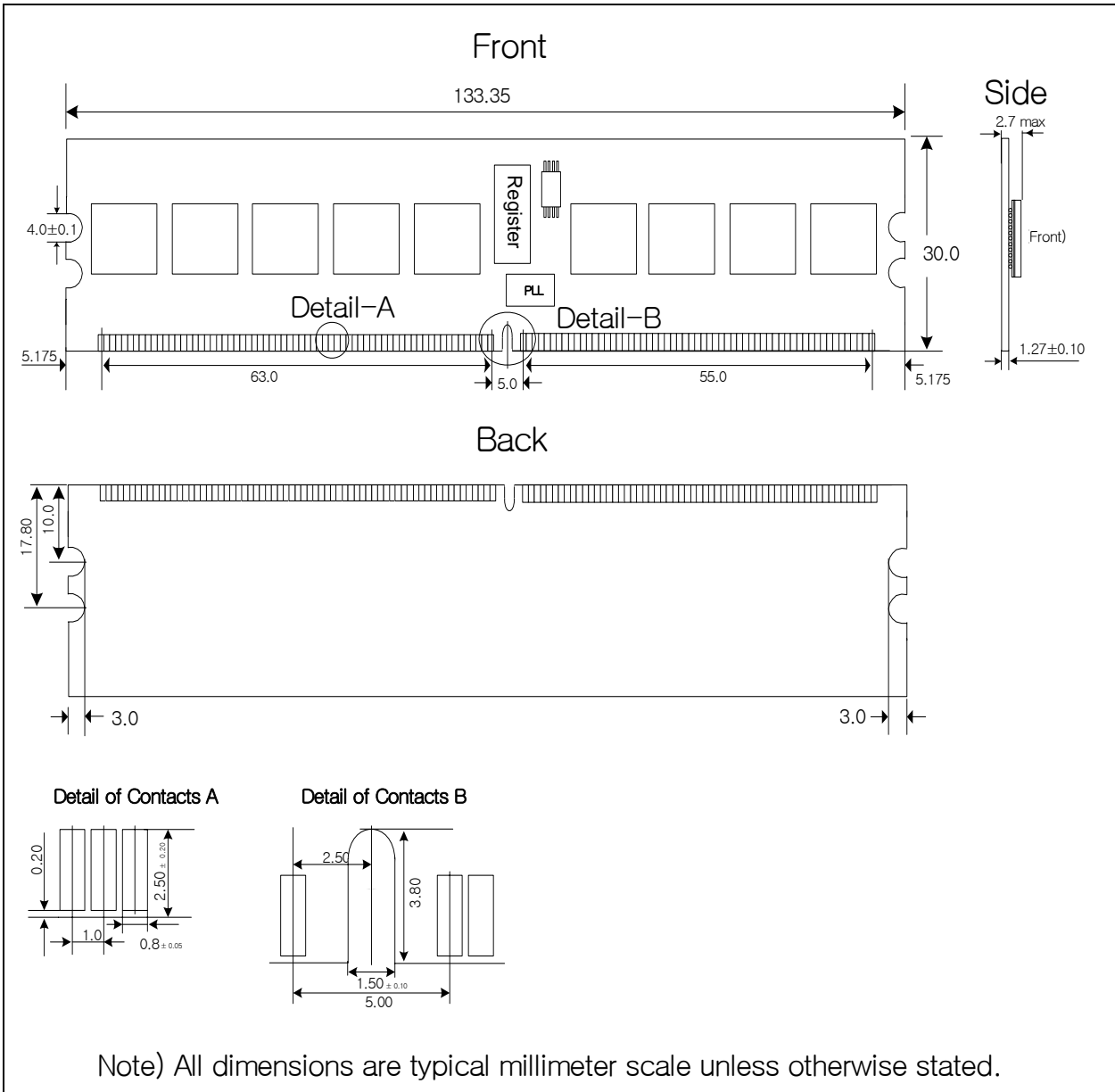
1. For details and notes, please refer to the relevant HYNIX component datasheet (HY5PS12[4, 8]21BFP).

2. 0°C ≤ TCASE ≤ 85°C

3. 85°C < TCASE ≤ 95°C

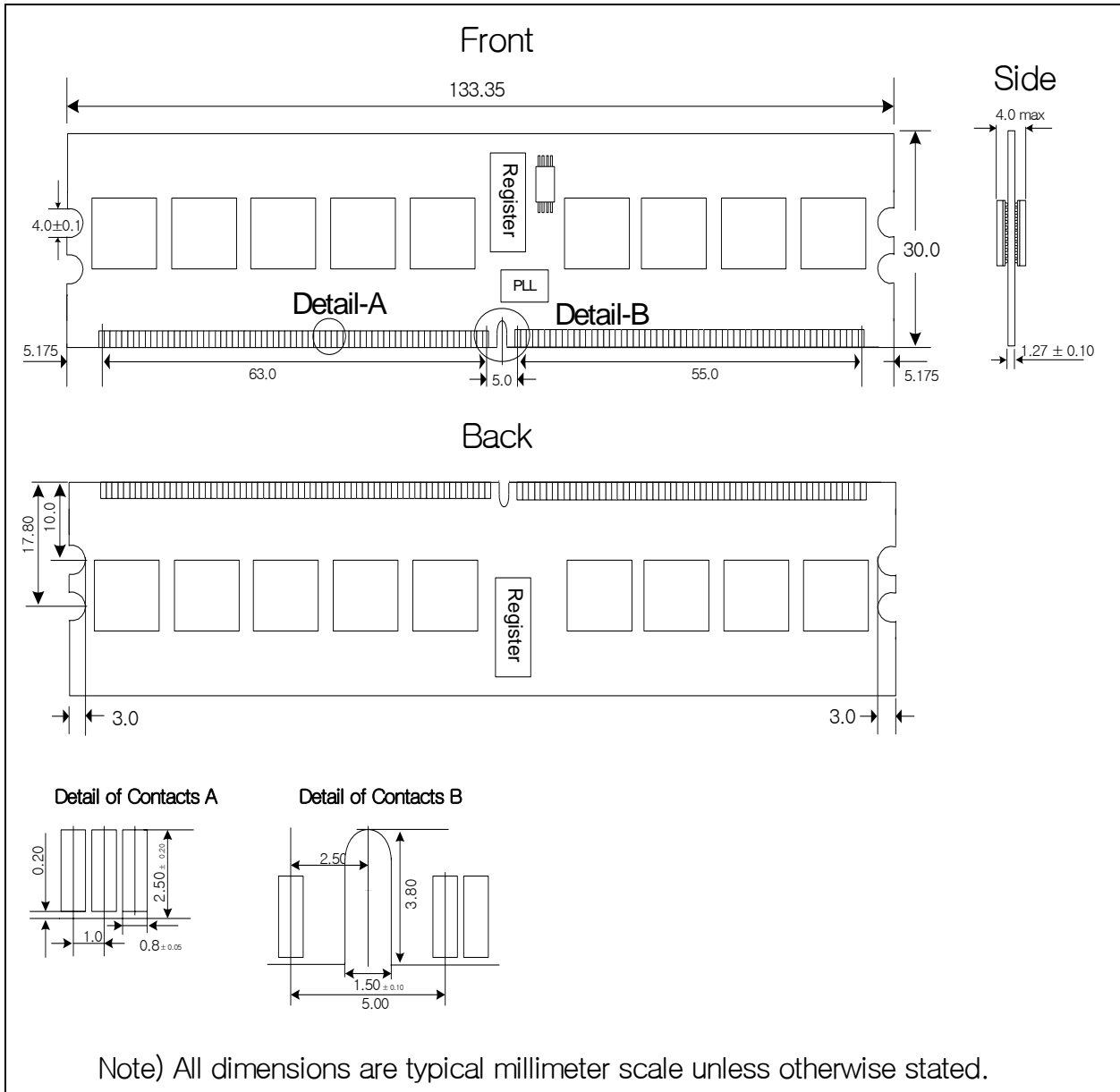
PACKAGE OUTLINE

64Mx72 (1 rank) - HYMP564R72BP8 / HYMP564P72BP8



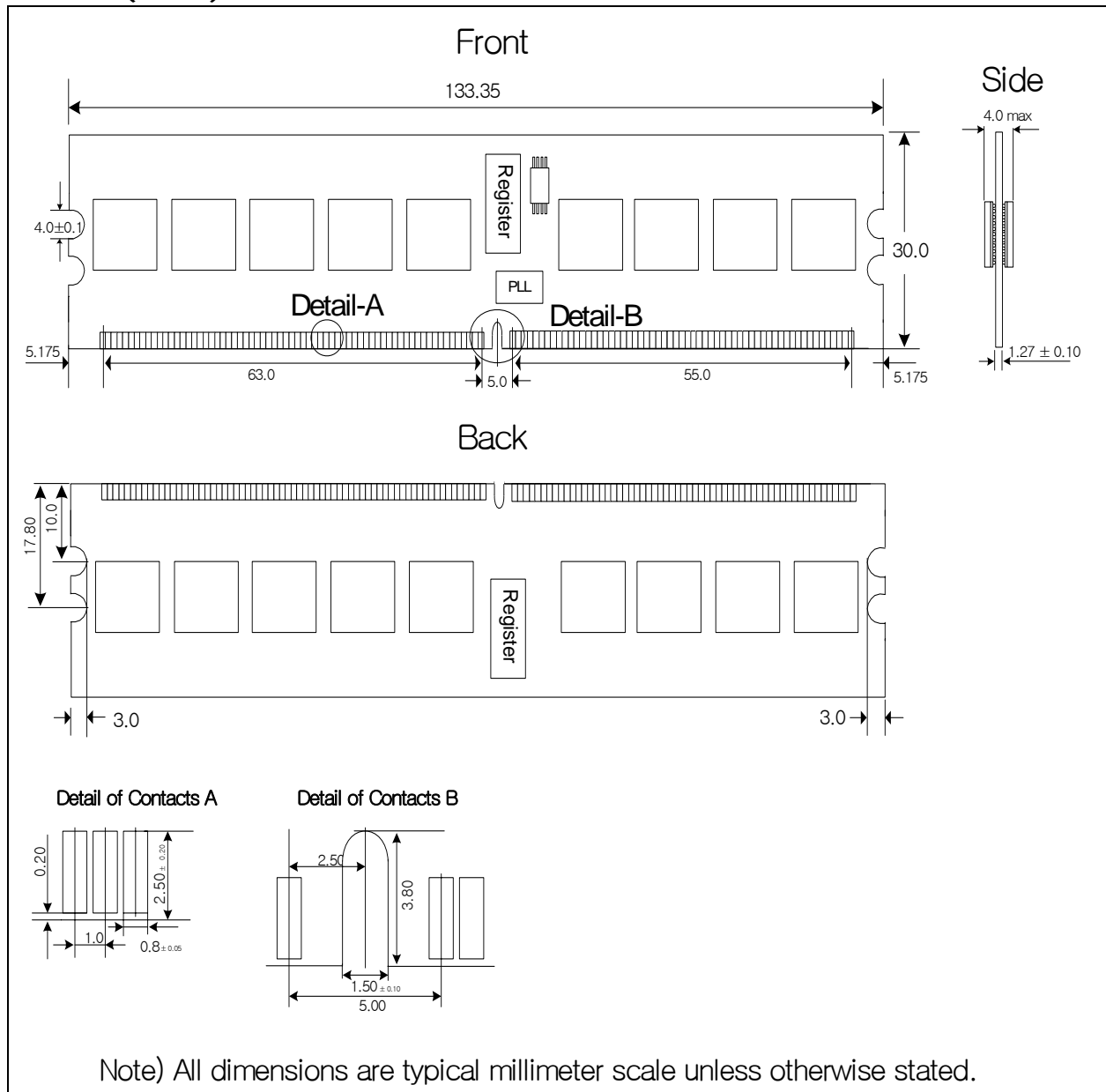
PACKAGE OUTLINE

128Mx72 (2 ranks) - HYMP512R72BP8 / HYMP512P72BP8



**PACKAGE OUTLINE**

128Mx72 (1 rank) - HYMP512R72BP4 / HYMP512P72BP4







## REVISION HISTORY

Revision	History	Date	Remark
1.0	First Version Release	Oct. 2005	
1.1	Leakage current spec. added to the DC OPERATING CONDITIONS	July 2006	